9 Schematic Diagrams
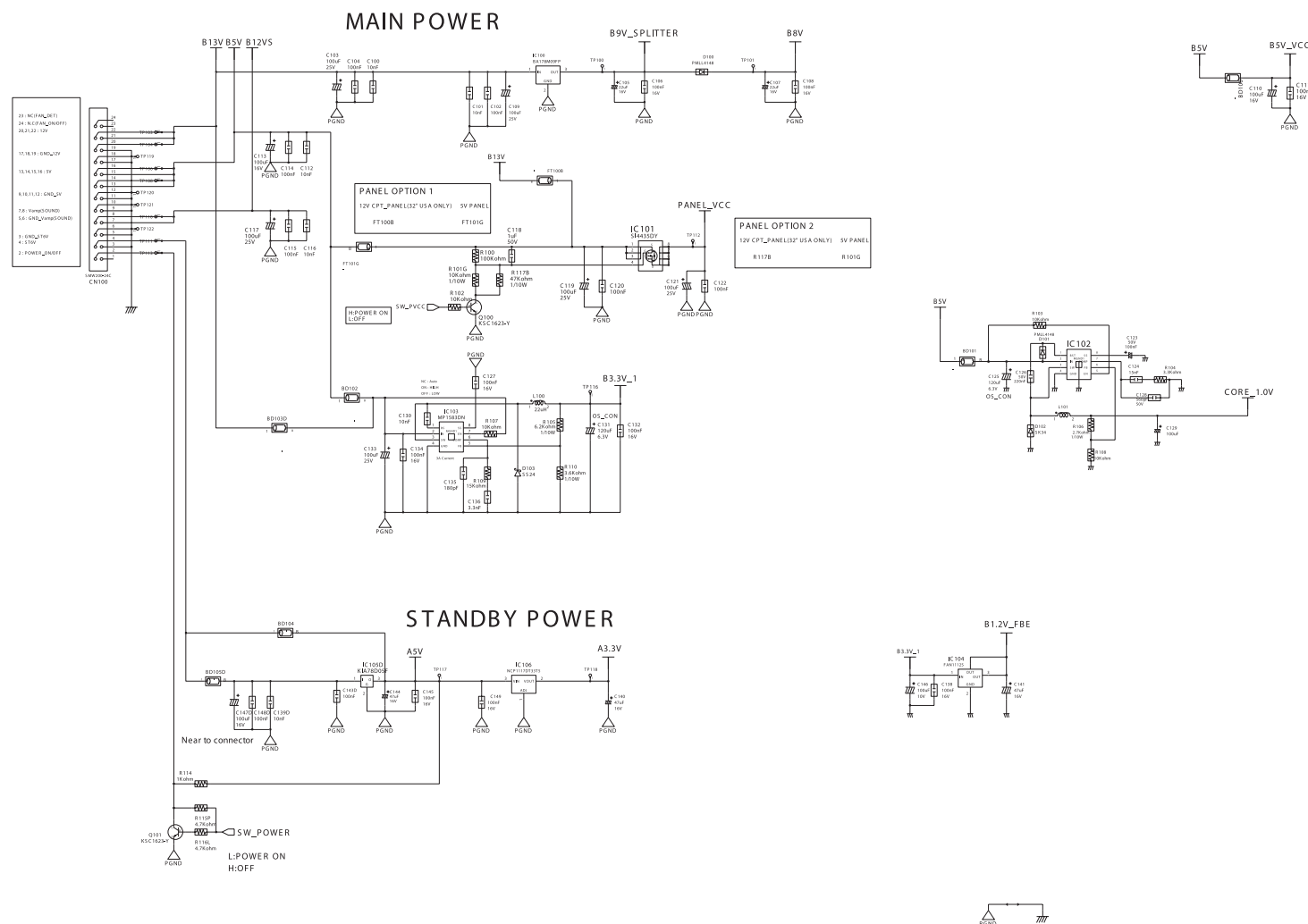
- This Document can not be used without Samsung s authorization.
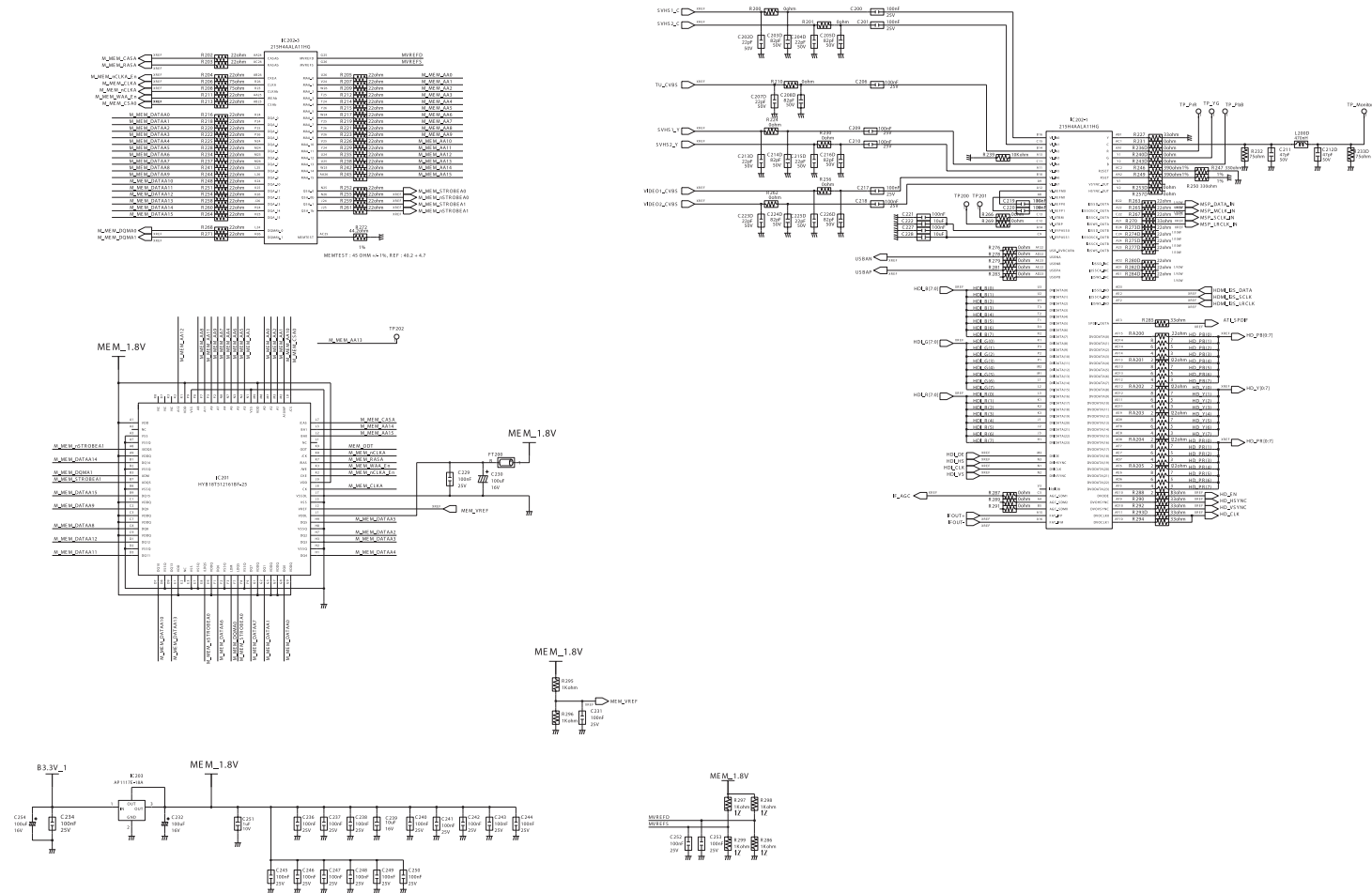
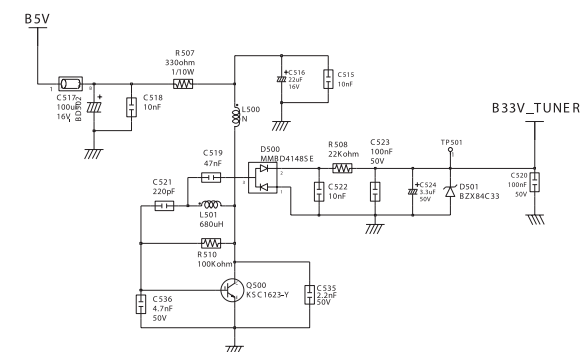## 9-1 MAIN POWER BLOCK Schematic Diagram (N36A)

9-2 X242 INOUT MEMORY Schematic Diagram (N36A)

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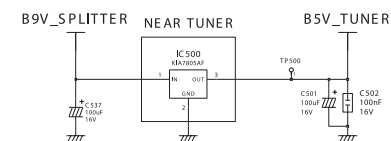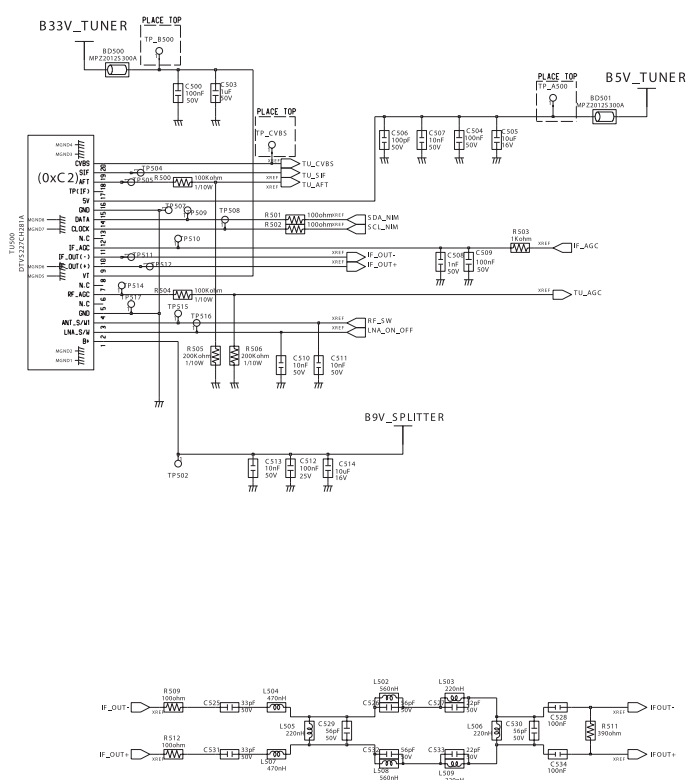
9-3 X242 INOUT MEMORY Schematic Diagram (N36A)
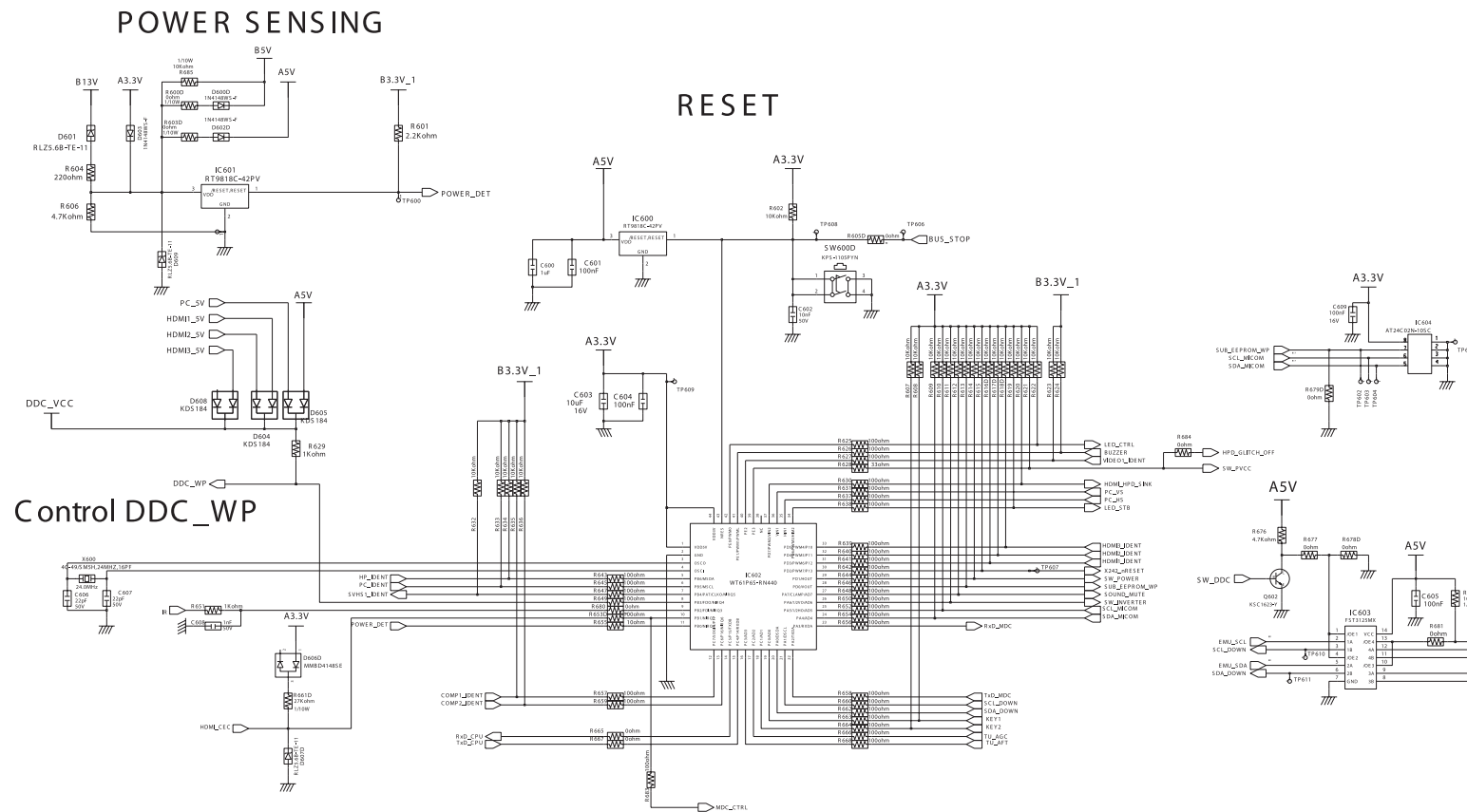
9-4 X242 POWER Schematic Diagram (N36A)

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9-5 TUNER & SPLITT Schmetic Diagram (N36A)
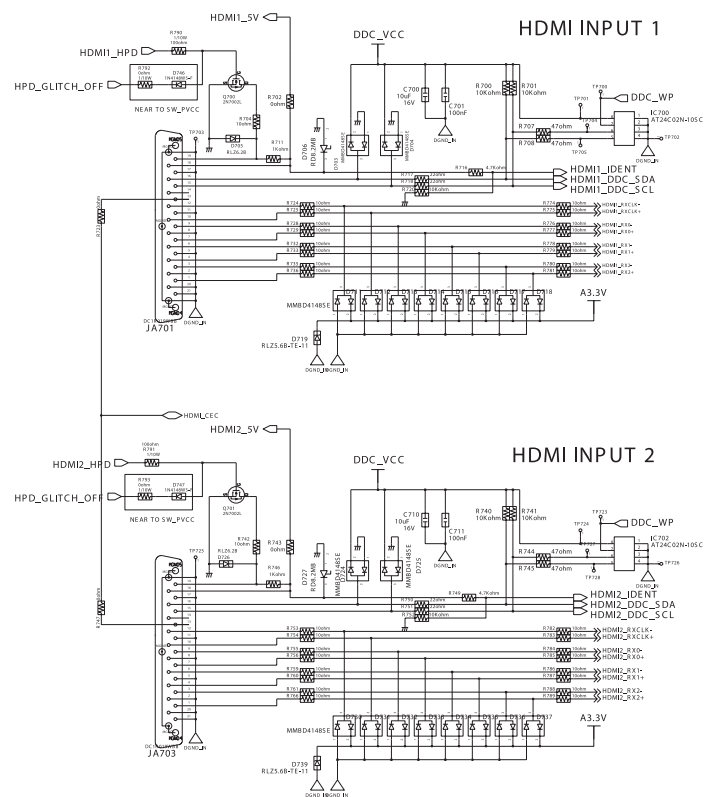

ATSC HALF NIM TUNER

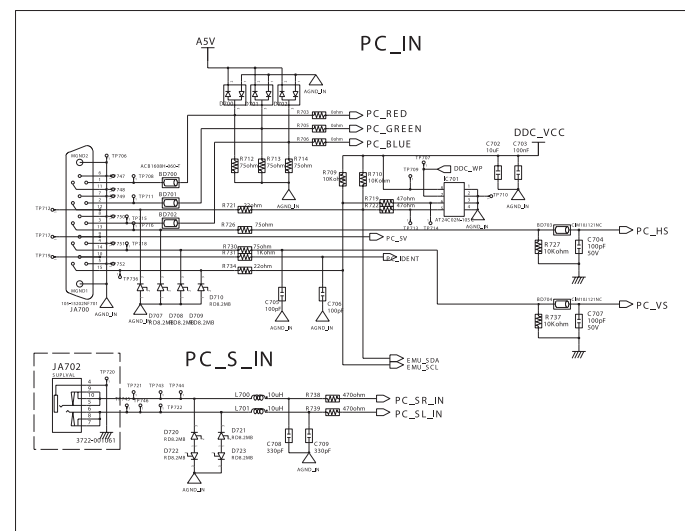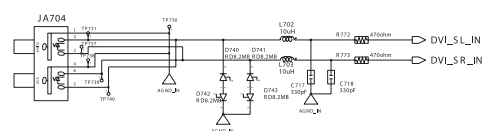- This Document can not be used without Samsung s authorization.

9-6 STANDBY MICOM (WT61P6S) (N36A)

POWER SENSING

RESET

Control DDC_WP

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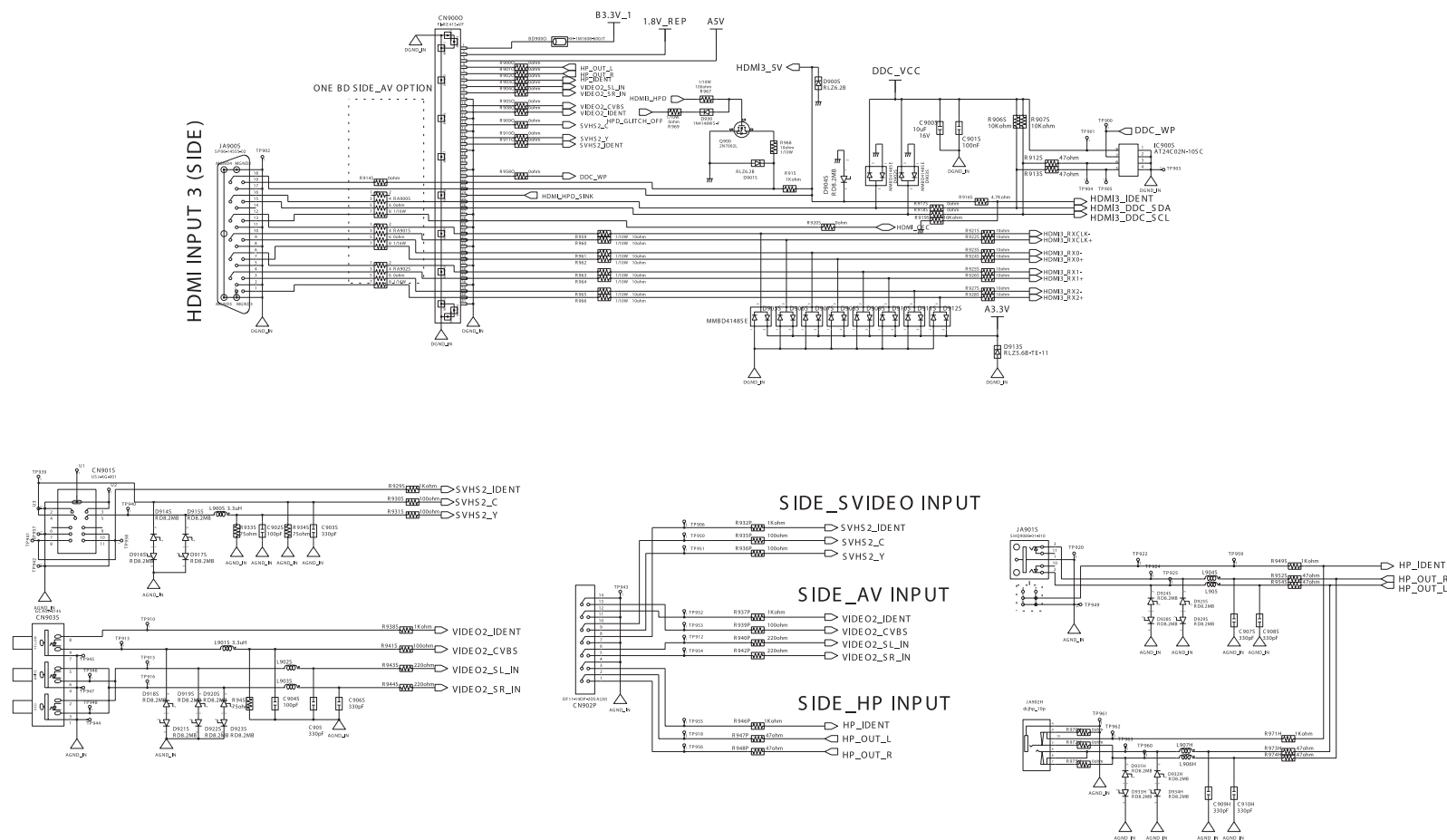
9-7 PC & HDMI INPUT Schmetic Diagram (N36A)

HDMI INPUT 1

HDMI INPUT 2

DVI SOUND INPUT

PC_IN

PC_S_IN

USB Download

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9-8 AV INPUT / OUTPUT Schmetic Diagram (N36A)
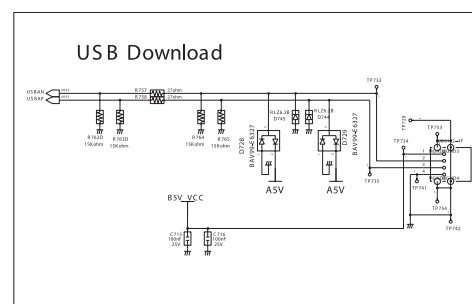
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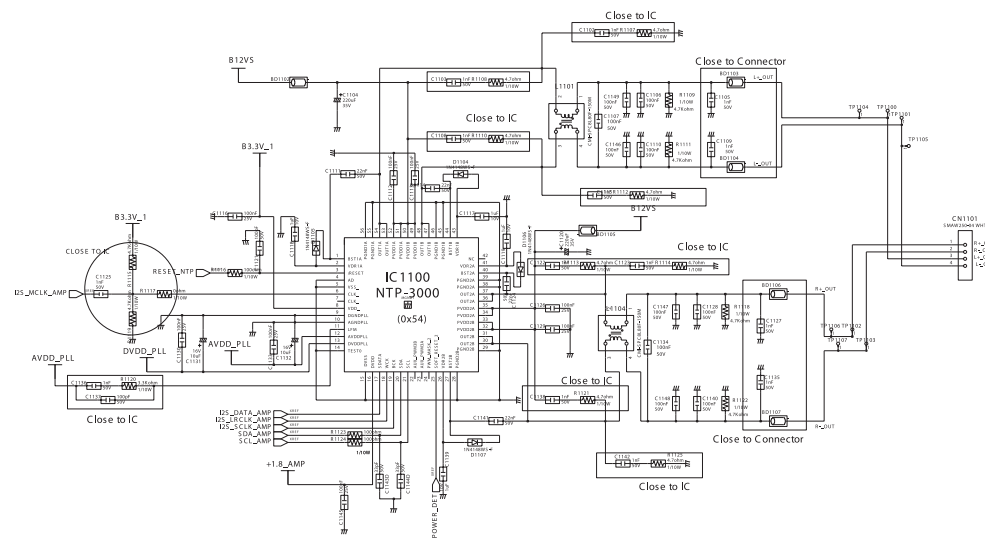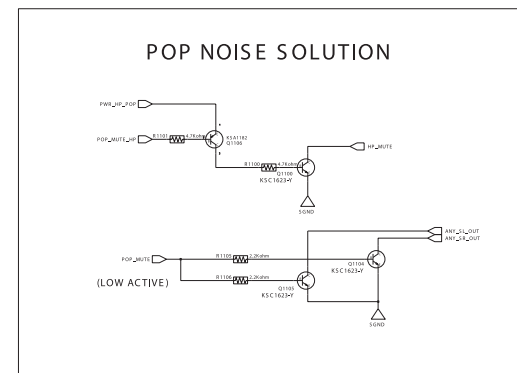## 9-9 SIDE AV (N36A)

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9-10 MSP4450K Schmetic Diagram (N36A)
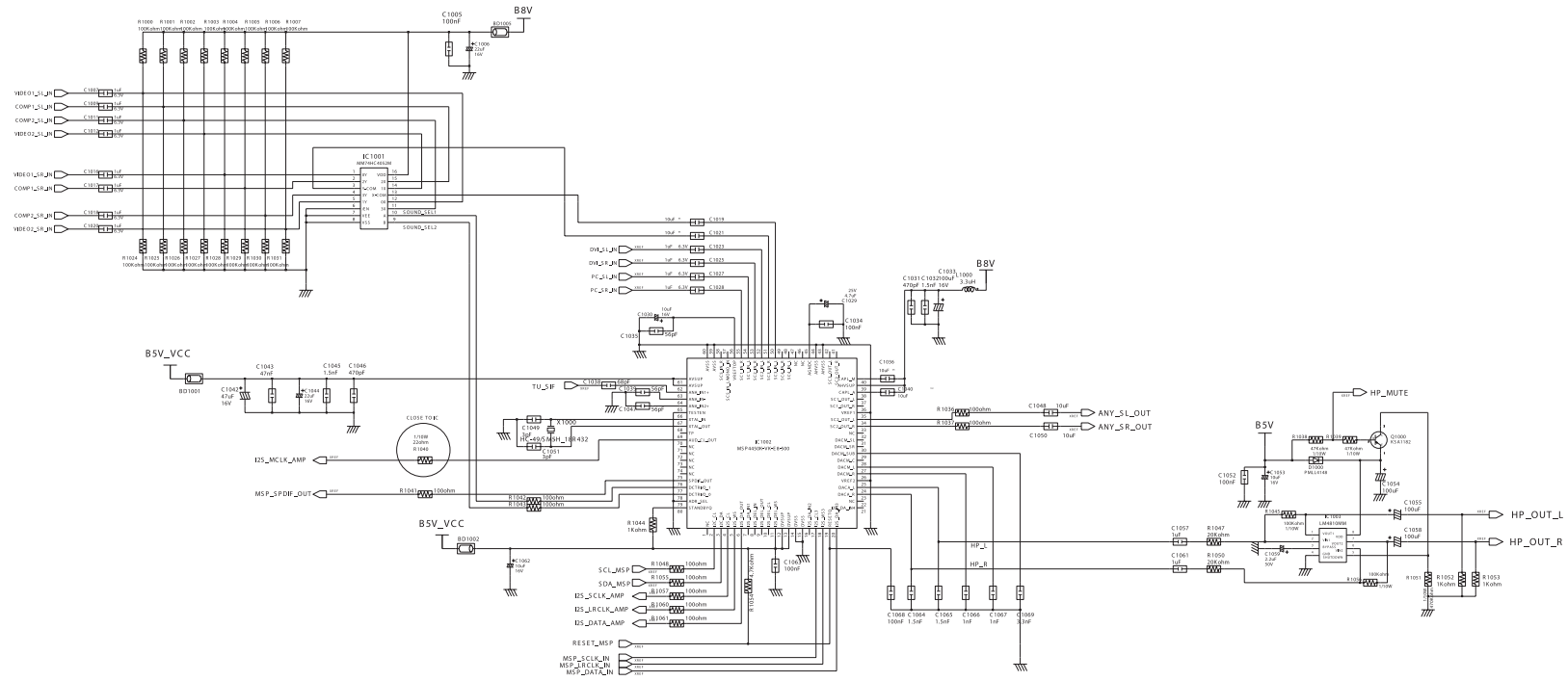
9-11 SOUND AMP(NTP3000) Schmetic Diagram (N36A)
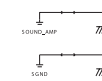
POP NOISE SOLUTION

9-12 MST3388 & SIL9185 Schmetic Diagram (N36A)

ADC + HDMI[MST3388]

IC1201
MST3388MK-LF-110

I2C ADDR SEL

		R1239	R1237
PHY CTRL	D0	D4
EDID	E0	E0
CEC	C0	C4

HDMI SWITCH

R1247 : I2C MODE

R1246D : STAND ALONE MODE

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9-13 FBE (N36A)

9-14 SUB-FUNCTION Schmetic Diagram (N36A)
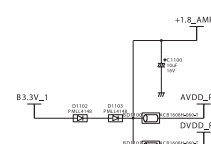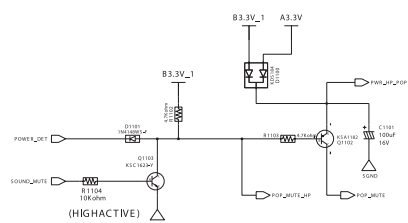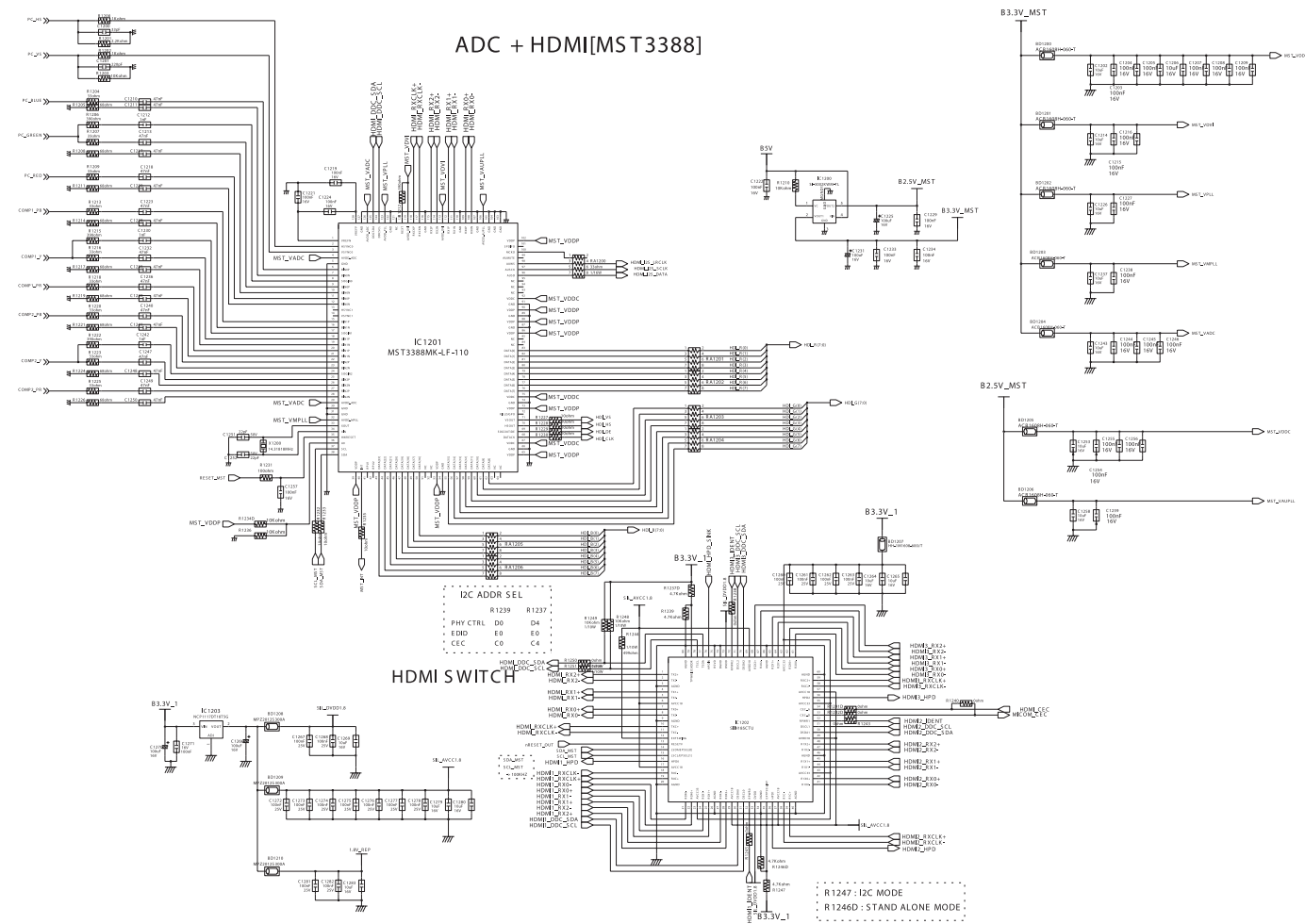
SUB FUNCTION I/F
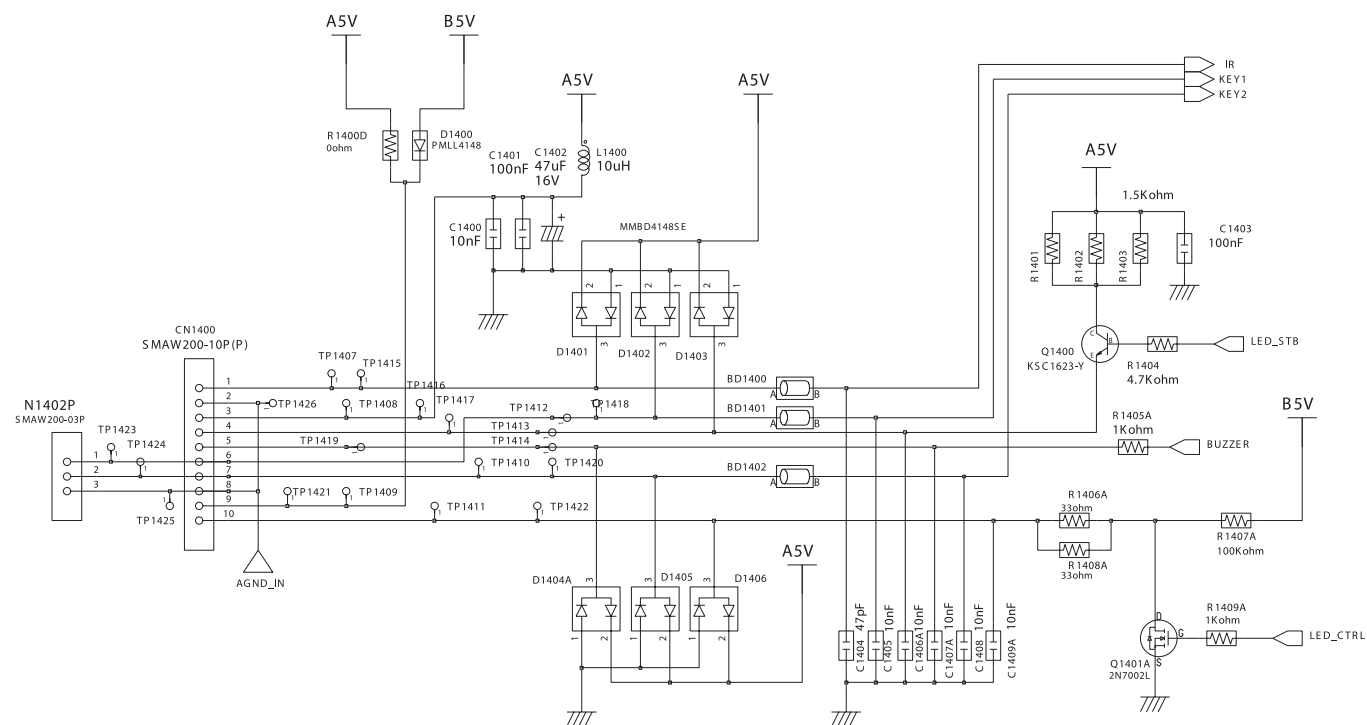
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9-15 MAIN POWER BLOCK Schematic Diagram (N34B)

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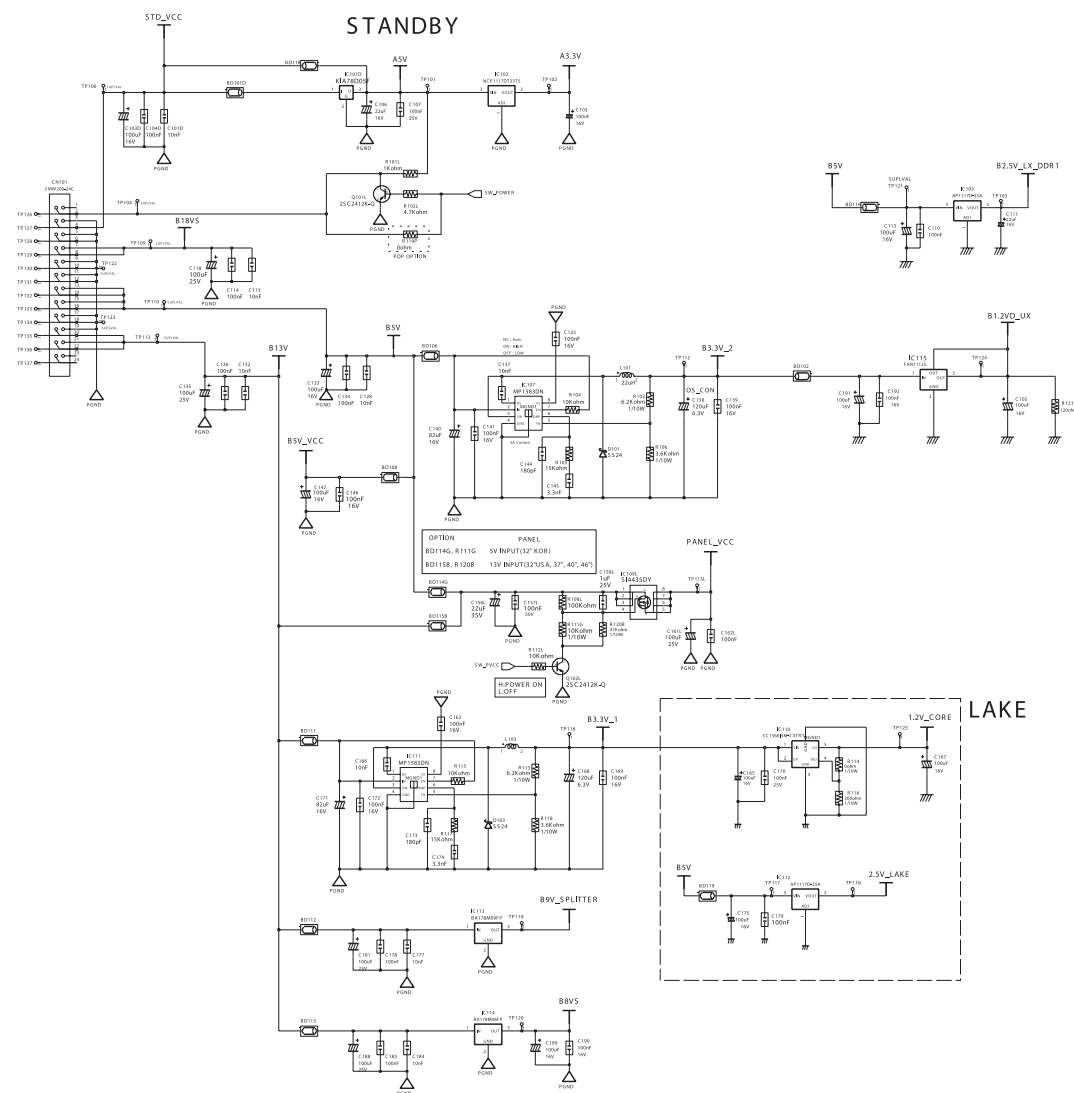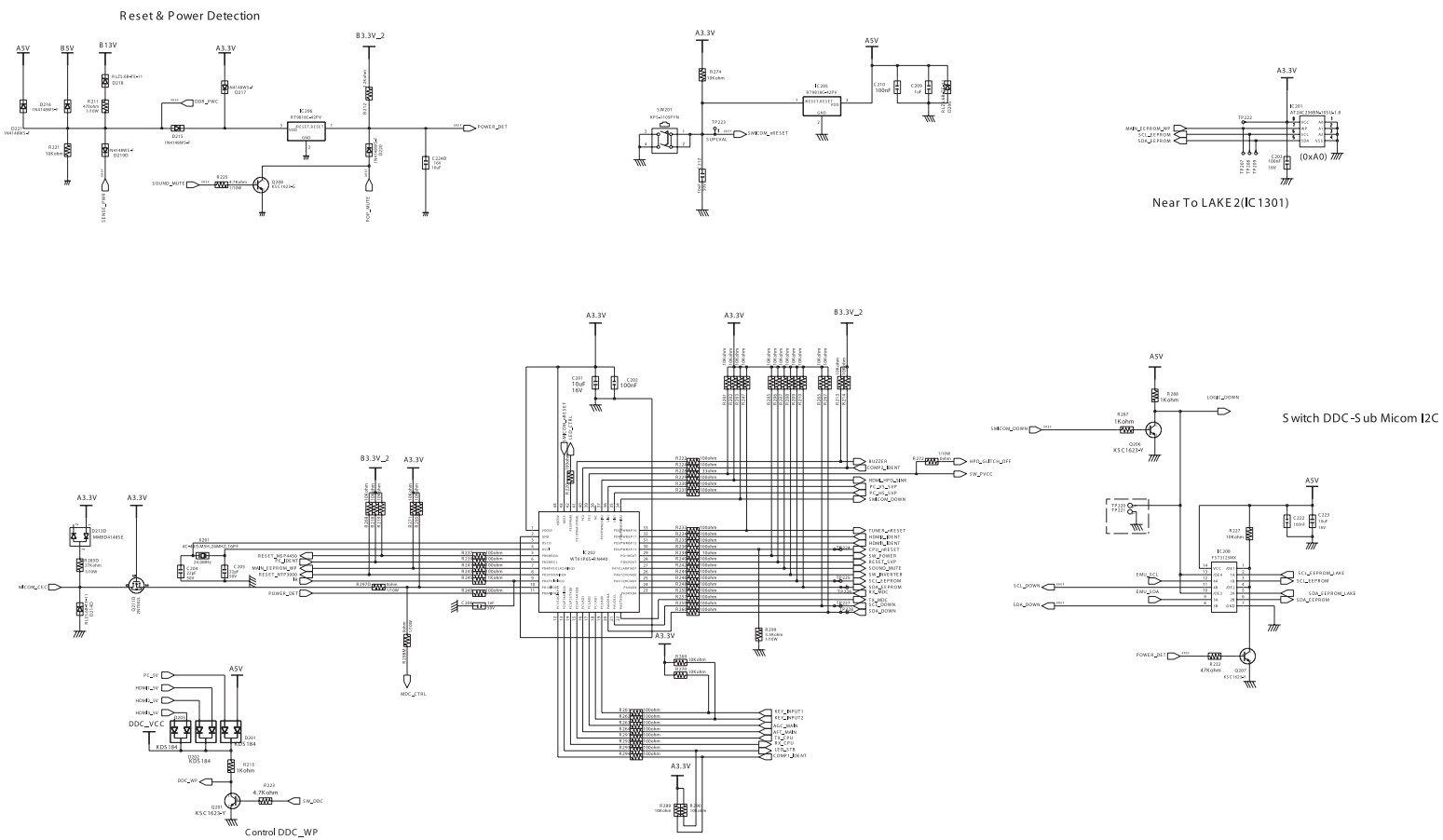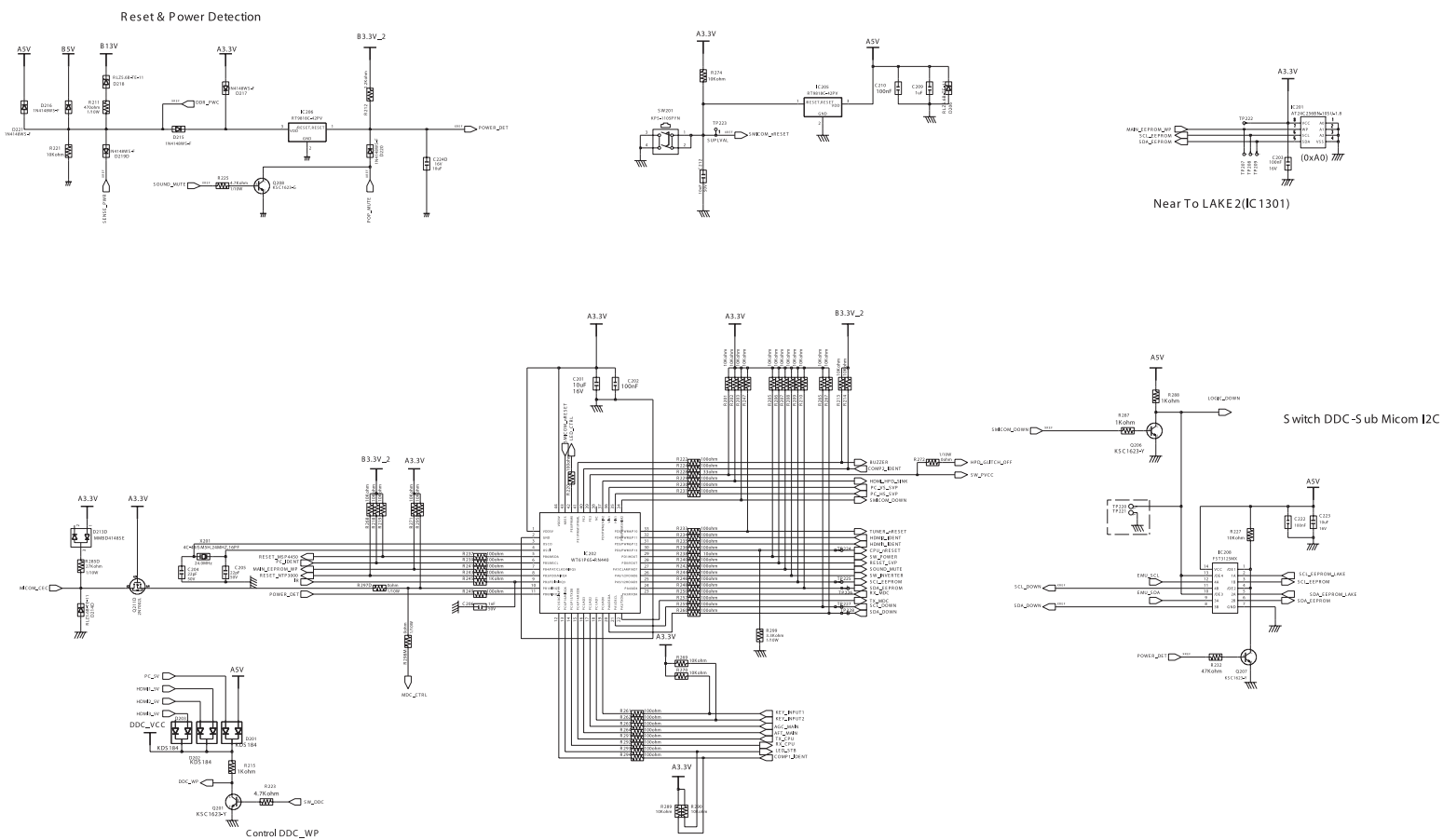
9-16 STANDBY MICOM (WT61P6) Schematic Diagram (N34B)

Reset & Power Detection

Near To LAKE 2(IC1301)

Switch DDC-Sub Micom I2C

Control DDC_WP

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9-17 SOUND PROCESSOR (MSP4450) Schematic Diagram (N34B)

Reset & Power Detection

Near To LAKE2(IC1301)

Switch DDC-Sub Micom I2C

Control DDC_WP

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9-18 SOUND AMP (NTP3000) & POP SOLUTION Schematic Diagram (N34B)
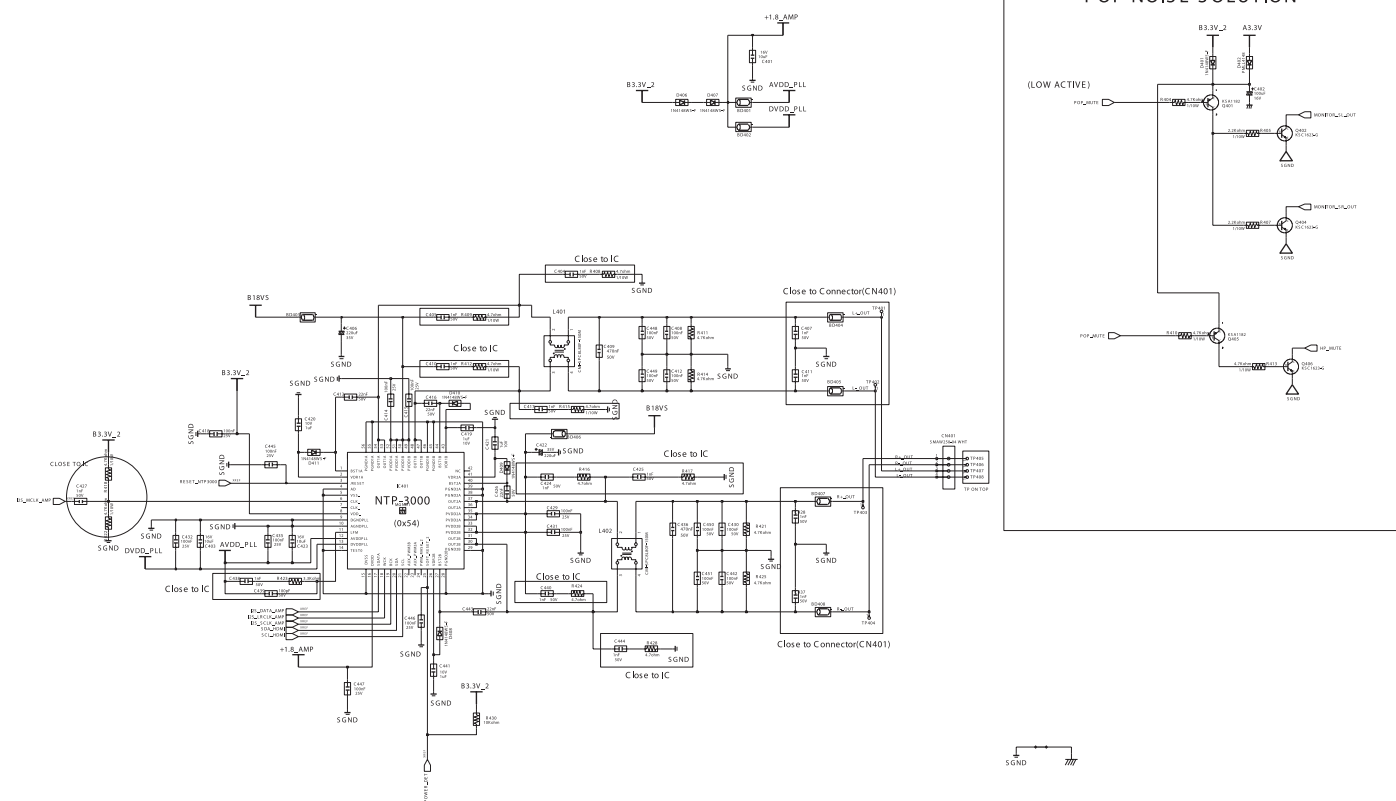
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9-19 NIM TUNER 1410 Schmetic Diagram (N34B)

ATSC HALF NIM TUNER

9-20 BACK AV IN / OUT Schmetic Diagram (N34B)
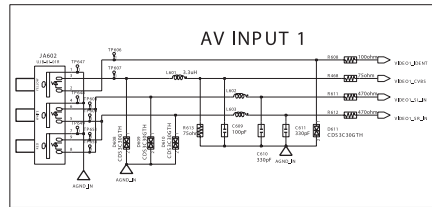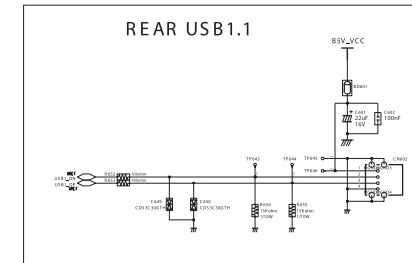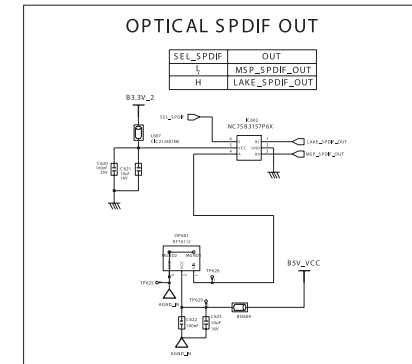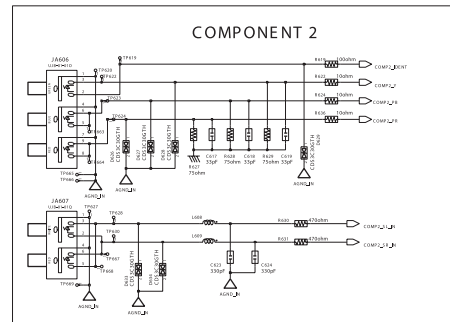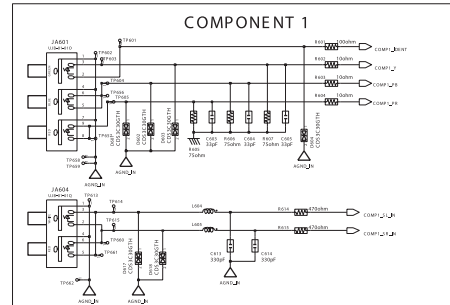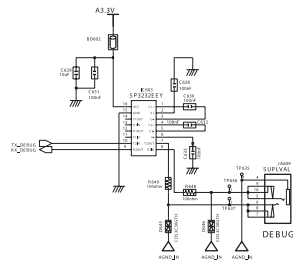
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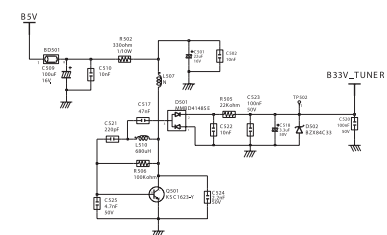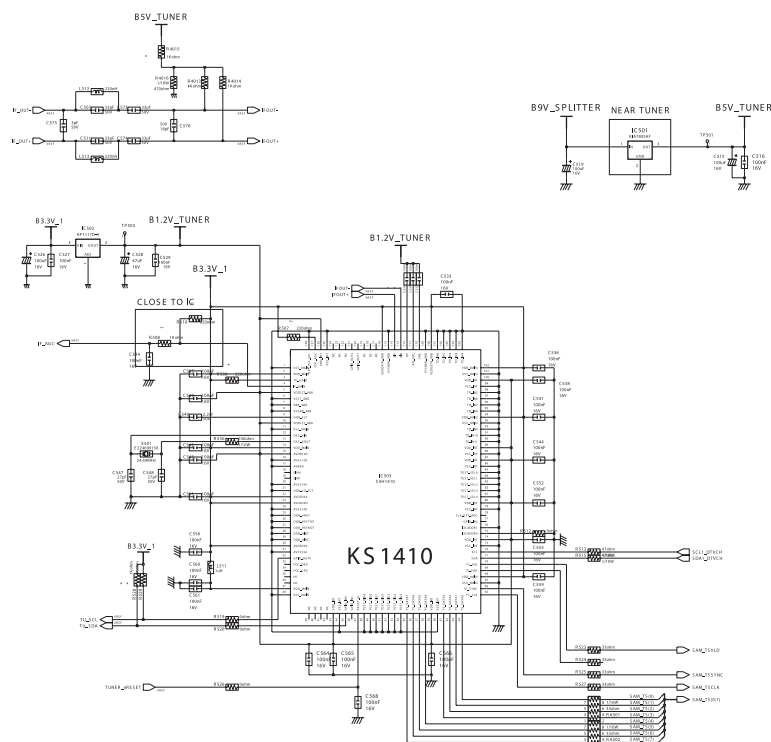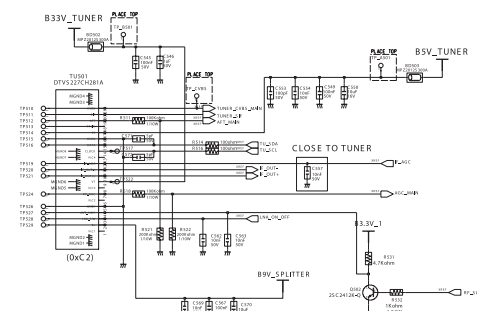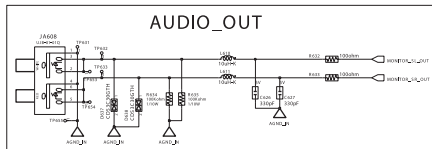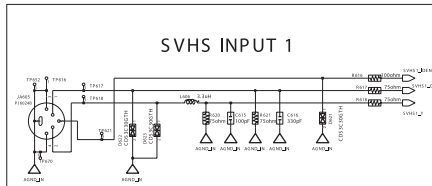
9-21 SIDE AV IN / OUT Schmetic Diagram (N34B)
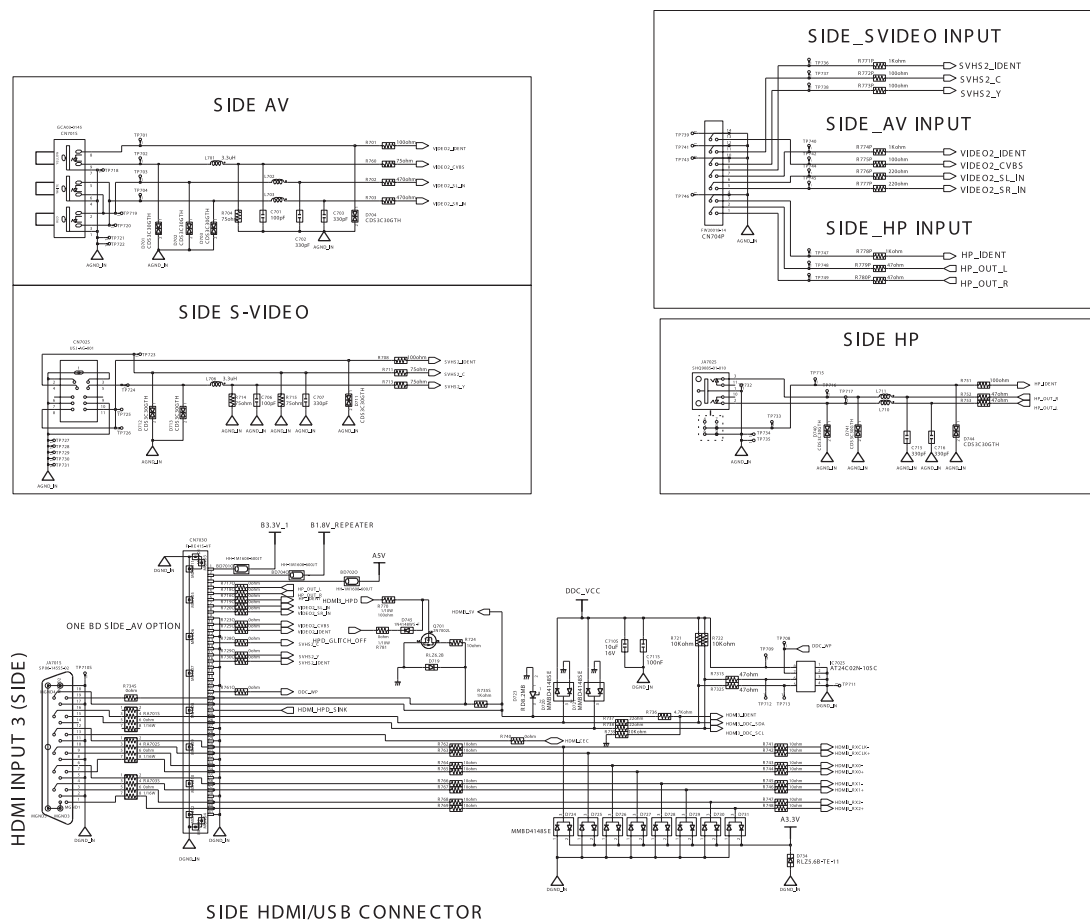
SIDE AV

SIDE S-VIDEO

SIDE_SVIDEO INPUT

SIDE_AV INPUT

SIDE_HP INPUT

SIDE HP

HDMI INPUT 3 (SIDE)

ONE BD SIDE_AV OPTION

SIDE HDMI/USB CONNECTOR

9-22 HDMI SWITCH & PC & HDMI INPUT Schmetic Diagram (N34B)

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9-23 SVP-PX POWER BLOCK Schmetic Diagram (N34B)

SVP_PX_POWER
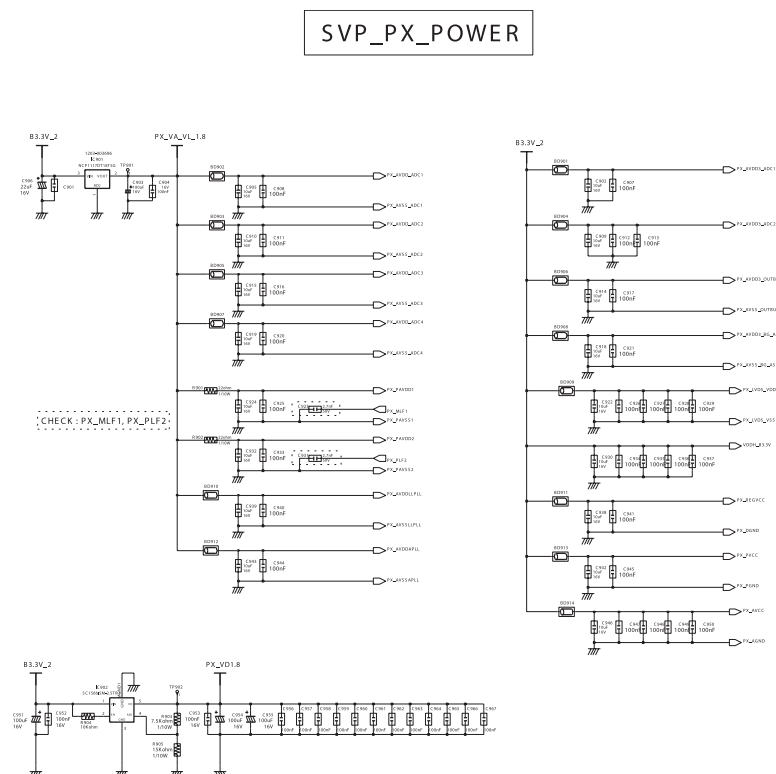
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9-24 VIDEO DECODER & SCALER (SVP-PX) Schmetic Diagram (N34B)

SVP-PX56-7256

NEAR TO PIN

*** HEAT SINK
—> BP62-00017A

I2C Chip Debug

WS	low
SD0	high
SCK	low

* DEL : R1020, R1021, R1023

BOOT STRAP		
Pin Name	HIGH	LOW
WS	Use ALE to latch address	Use falling edges of WR# & RD# to latch address
SD0	Use rising edge of WR# to latch data	Use falling edge of WR# to latch data
SCK	I2C Slave address = 0x7E./7F	I2C Slave address = 0x7C./7D

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9-25 SVP-UX DDR MEMORY Schmetic Diagram (N34B)

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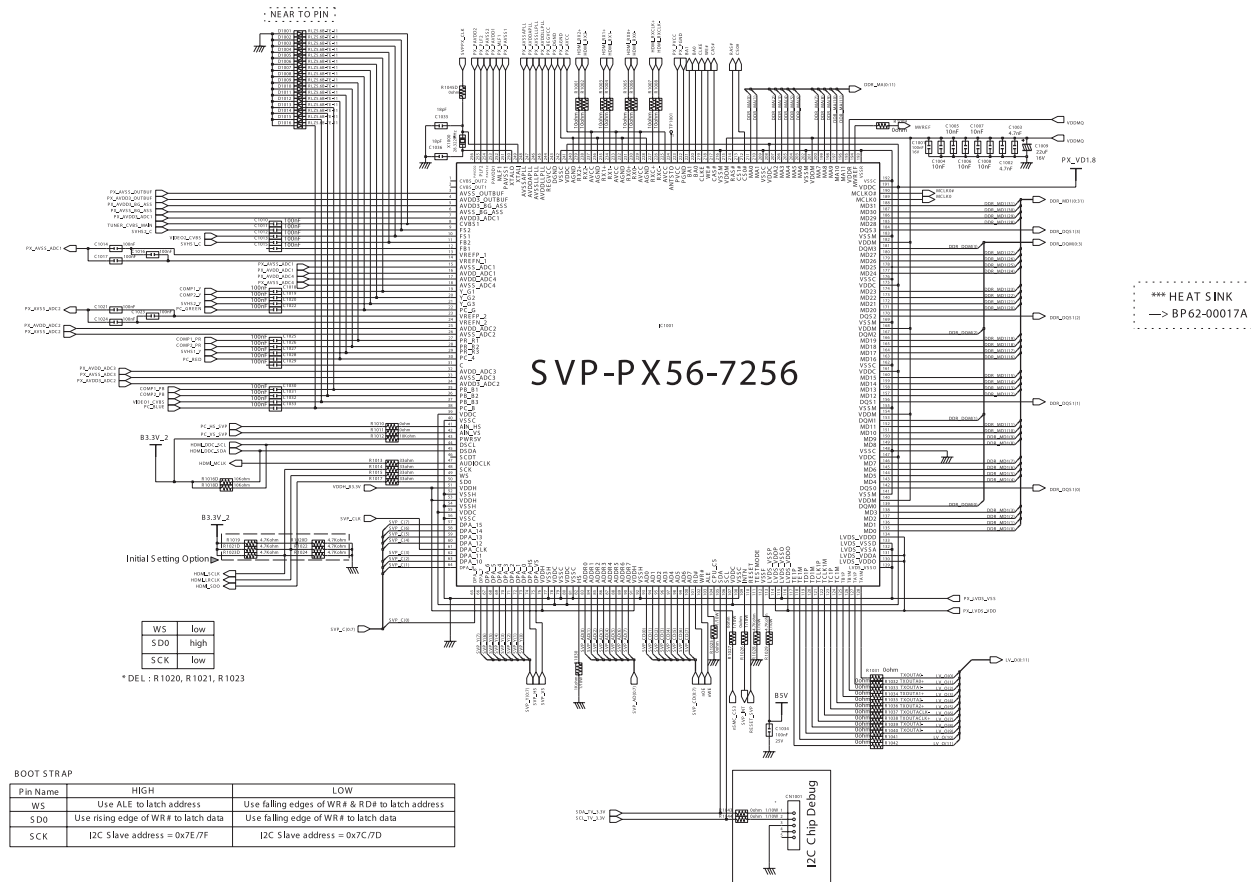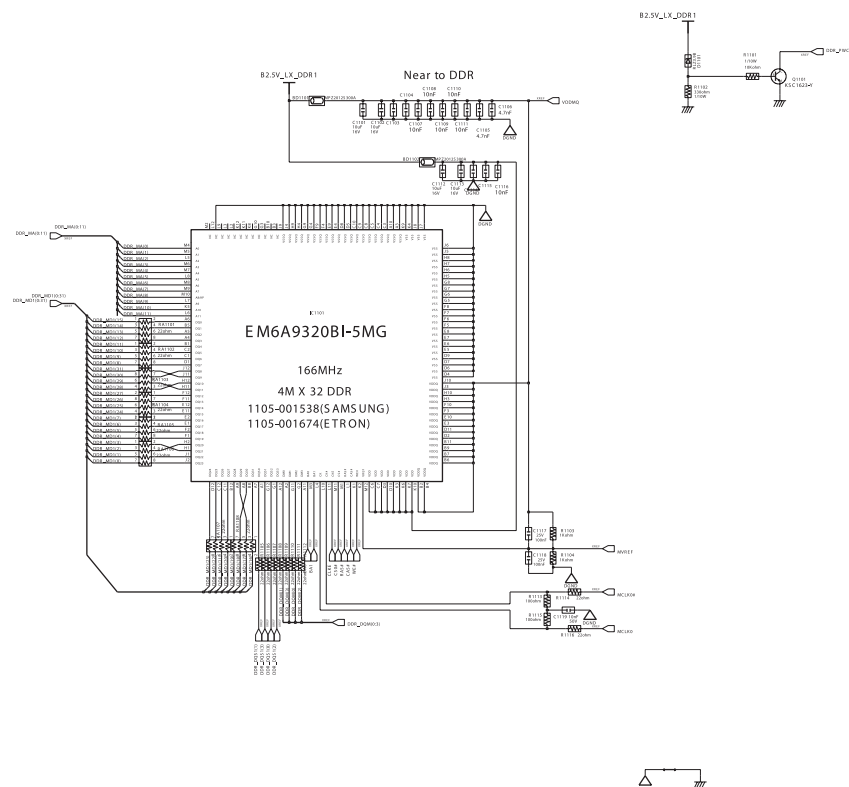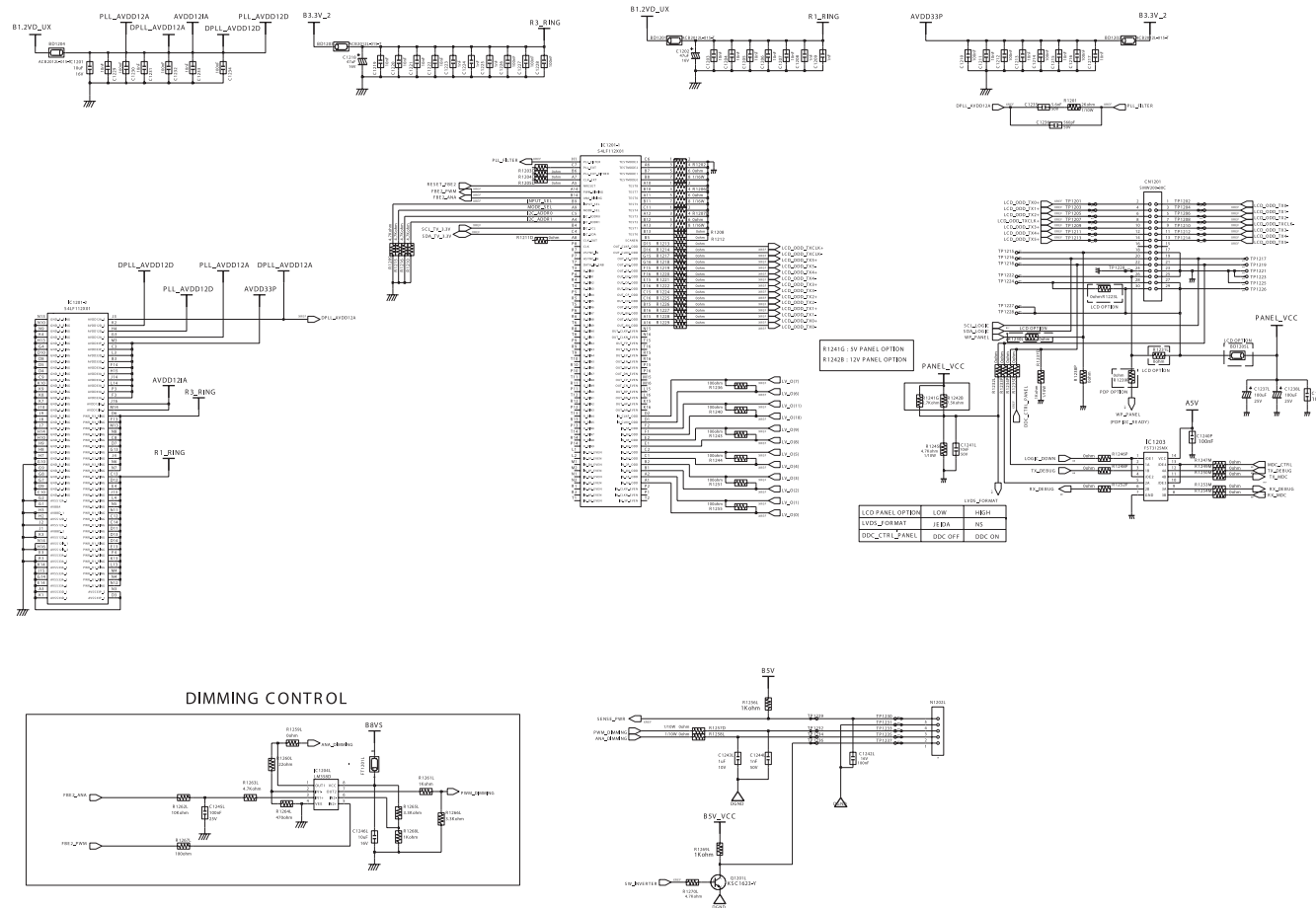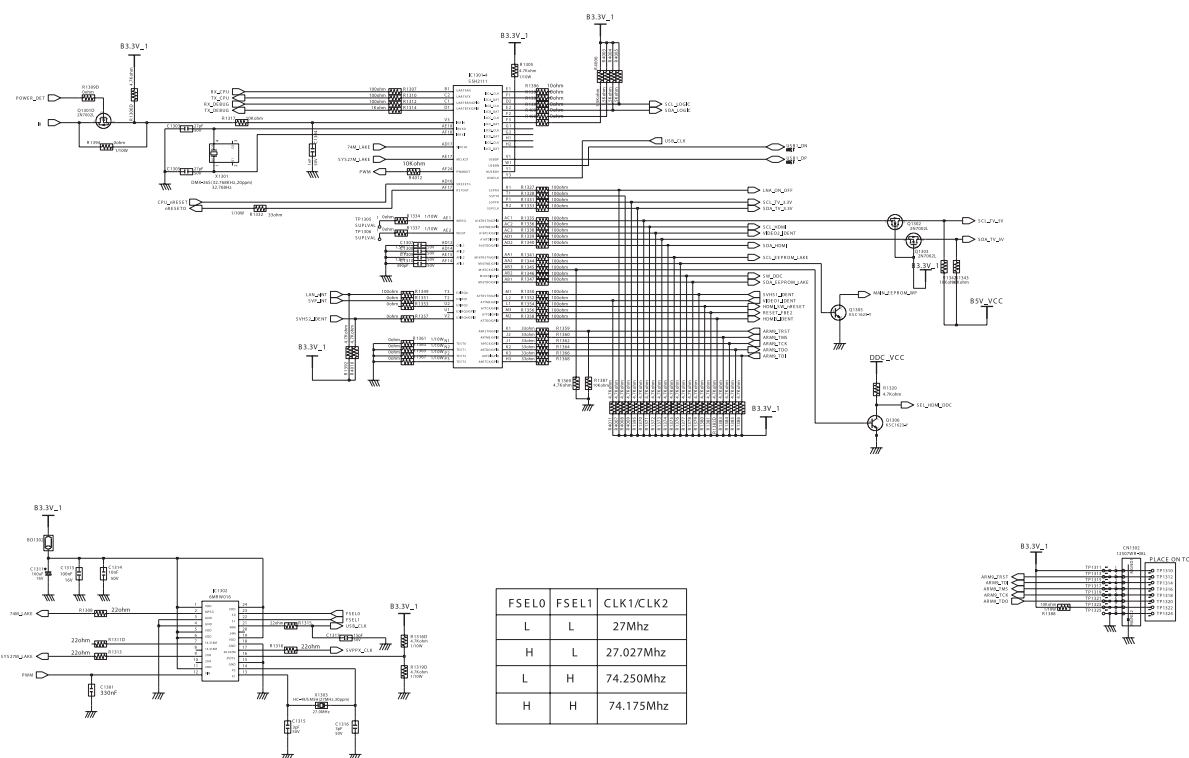## 9-26 LVDS & PWM CONTROL & PANEL I/F Schmetic Diagram (N34B)

DIMMING CONTROL

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9-27 LAKE (I2C & GPIO & USB & UART & INT) Schmetic Diagram (N34B)

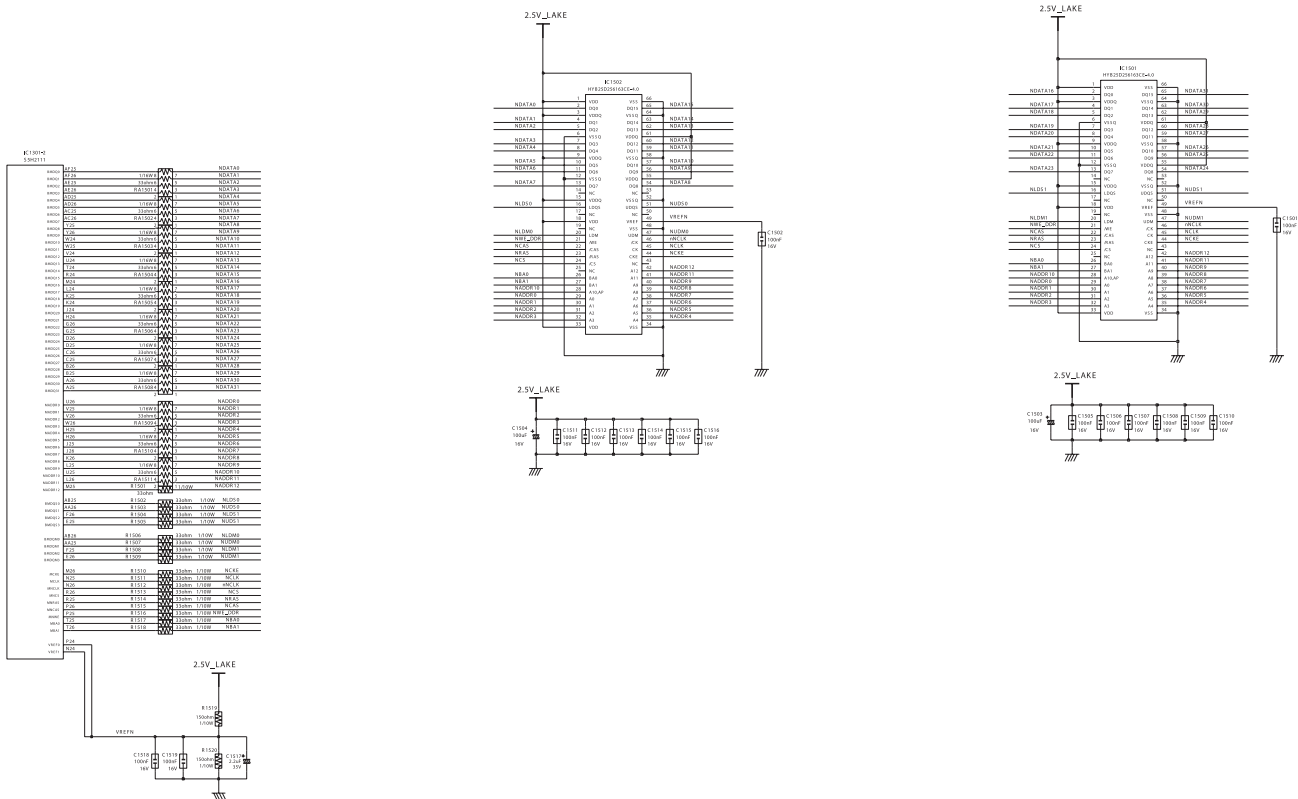| FSEL0	FSEL1	CLK1/CLK2
L	L	27Mhz
H	L	27.027Mhz
L	H	74.250Mhz
H	H	74.175Mhz

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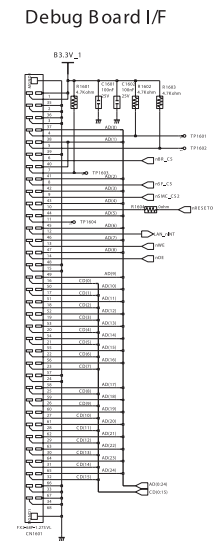## 9-28 LAKE (I2S IN/OUT & TS-IN & YCbCr-OUT) Schmetic Diagram (N34B)

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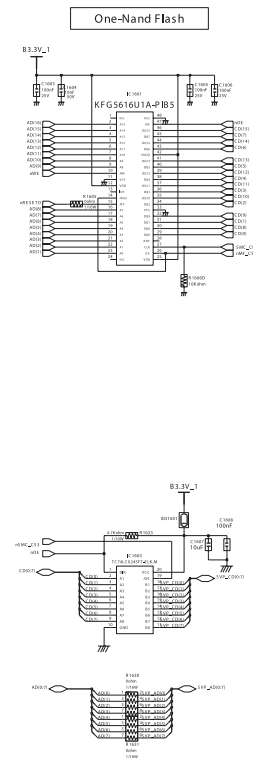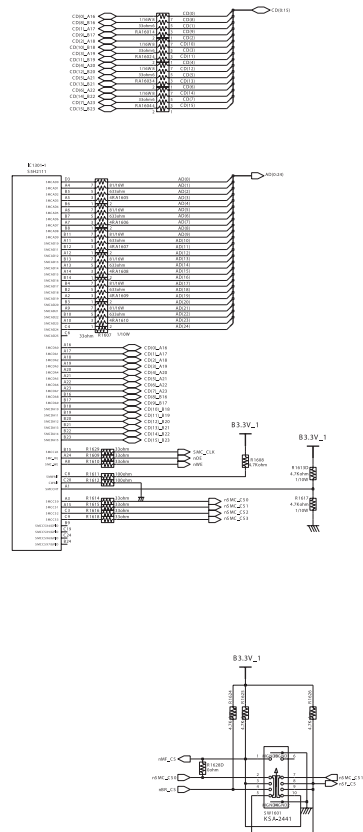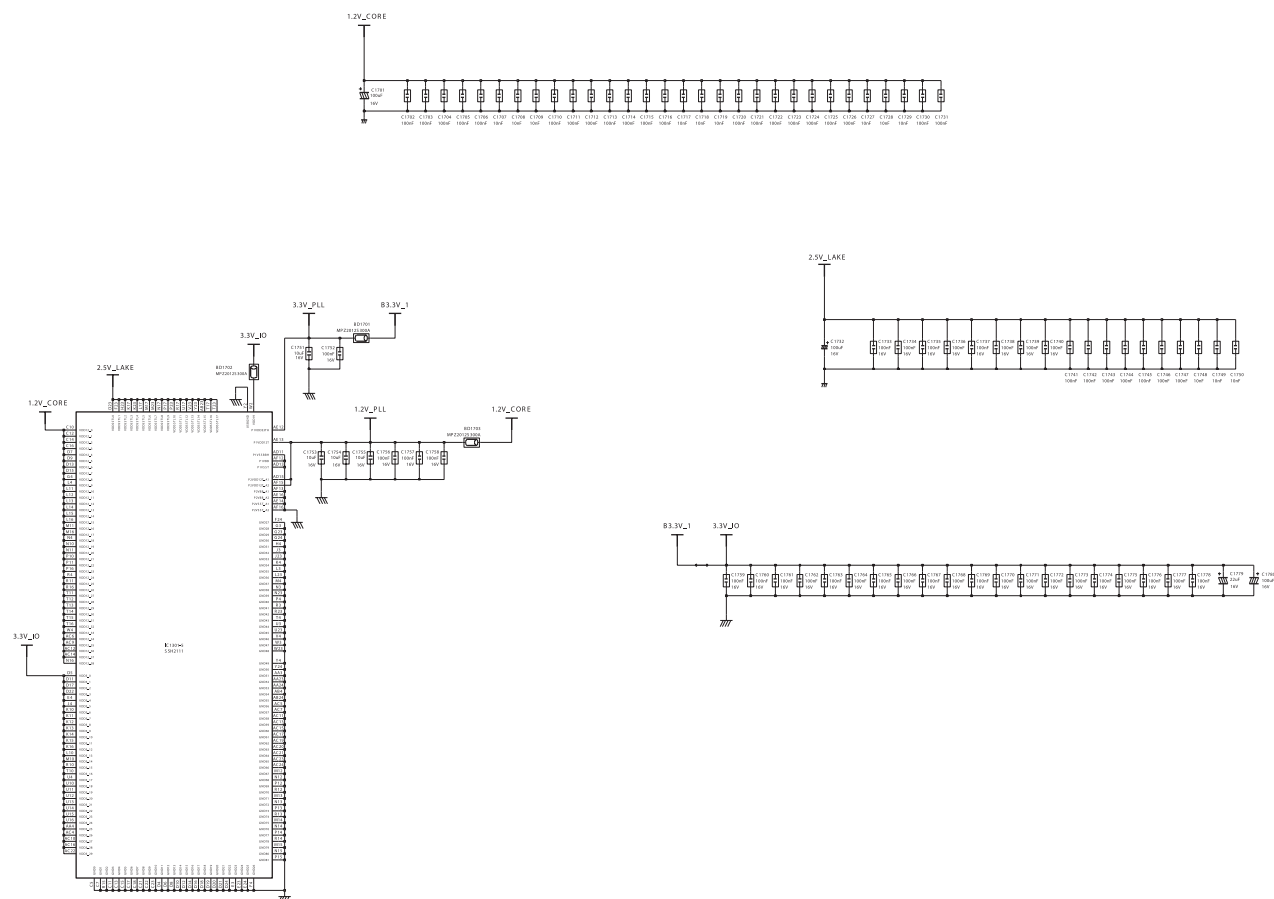
9-29 LAKE (DDR MEMORY) Schmetic Diagram (N34B)

9-30 LAKE (STATIC MEMORY & DEBUG) Schmetic Diagram (N34B)

One-Nand Flash

KFG5616U1A-PIB5

Debug Board I/F

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9-31 LAKE (POWER BLOCK) Schmetic Diagram (N34B)

9-32 SUB FUCNTION Schmetic Diagram (N34B)

SUB FUNCTION I/F